Analog Interface Card – A2D2A for Texas Instruments DSP Development Systems

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Abstract: The design of an interface card with eight analog inputs and four analog outputs is described in this technical paper. This card can be used with any Texas Instruments TI320 DSP development system. The A2D2A generates all of the necessary voltages on board from the 5V power, which is available according to the TMS320 Cross-Platform Daughtercard Specifications. For an easy interface, the common BNC coaxial connectors are used for the input and output connections. To reduce the manufacturing costs, the card has been designed using a two layer PCB.

Keywords: DSP development system, Cross-Platform Daughtercard

1 Introduction

Signal processing and control algorithms have increased in complexity since their introduction in the 1960's. The main research tools that have contributed to the development of these algorithms are simulation tools such as matlab from The MathWorks. Although these tools have become increasingly sophisticated, the evaluation of the proposed algorithms can only be performed through real-time experiments.

The implementation of signal processing and control algorithms in real-time experiments has become more feasible with the introduction of Digital Signal Processors (DSP). For implementation, it is required that these DSPs be constructed in the form of embedded systems. On the market, more than one system is available with the ability to perform either general or specific functions. These systems are frequently characterized by high price and a low lifespan, due to their fast evolution. Fortunately, all the DSP manufacturers sell their DSPs in the form of a development system, consisting of a minimal hardware and a development software bundle at an affordable price. Although the supplied hardware enables real-time algorithm development, the required connection to the analog world is seldom included. In order to overcome this problem, the DSP development boards are equipped with expansion connectors which allow the attachment of daughter cards.

2 A2D2A Card

In the following, the A2D2A interface card is described, which can be used by Texas Instruments development systems. This document is written not only with the intention to describe the developed A2D2A analog interface card but also with the objective is to present adequate information that aids the design of similar interface cards.

The A2D2A interface card, which facilitates communication between a TMS320 DSP development system and the analog environment, contains eight analog to digital (A/D) converter channels and four digital to analog (D/A) converter channels. For easy interfacing, the card uses common BNC coaxial connectors. The characteristic components of the interface card are listed in Table 1, while its block diagram is presented in Figure 1.

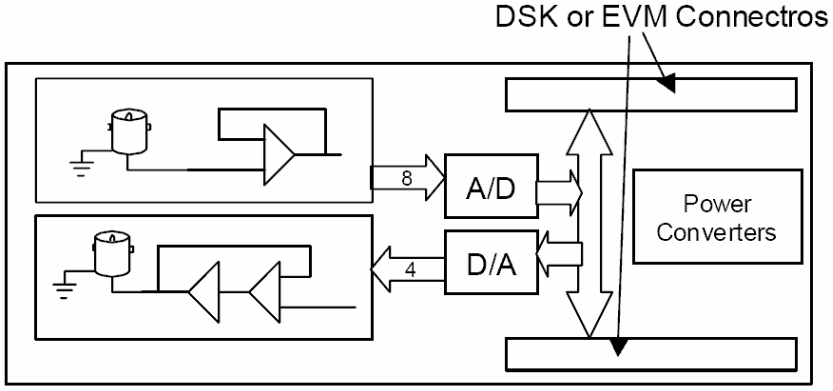

Figure 1
A2D2A: Block Representation

The top view of the A2D2A daughtercard is shown in Figure 2. The upper eight BNC connectors are the analog inputs while the lower four BNC connectors are the analog outputs. To prevent both mechanical and electrical damage to the card, the top surface does not contain electrical elements.

The A2D2A card offers eight channels of 14-bit A/D conversions and a sampling rate which can attain a frequency of 83kHz, as well as four channels of 16-bit D/A conversions, making it ideal for data acquisition in multidimensional signal processing, transient capture, and control systems.

Any sampling rate from 0 Hz to 83 kHz can be derived from the internal clock of the DSP. Due to the employed A/D converter, AD7865AS-1, from Analog Devices, all channels are sampled simultaneously with virtually zero phase delay.

Both the inputs and the outputs are equipped with appropriate amplifiers, which increase the input resistance and ensure the adequate output signal power.

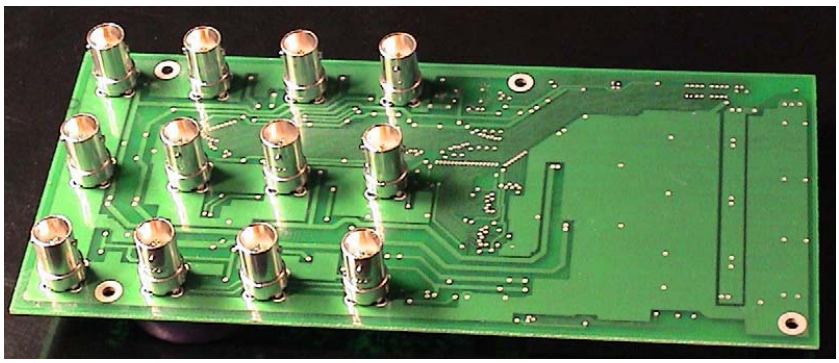

Figure 2
The top view of the A2D2A daughtercard

2 Description

One of the design objectives was to minimize the required interaction between the A2D2A card and the DSP. This was accomplished by the following manner. The timing of the A/D conversion is directly connected to the DSP's clock output. When the A/D conversion is complete, it generates an interrupt on the DSP. This is used to initiate a Direct Memory Access (DMA) transfer to read the converted data. At the end of the DMA transfer, a new interrupt is generated, which signals to the DSP that the A/D data is ready for processing. The D/A conversion control is further simplified when the write action automatically generates the D/A conversion. Next, the different units of the A2D2A card are described.

The timing of the A2D2A's conversion is initialized by a TOUT0 signal that is generated by the DSP's Timer 0. The resulting conversion lasts about 12μs. Following the completion of the conversion, an EXT_INT4 signal is generated. This signal is connected to the DSP's external interrupt line and generates an interrupt in the DSP, signaling that the data is ready for reading on the A2D2A card. The TOUT0 and the EXT_INT4 signals are the DSK's Peripheral Connector (J2) pins, 45 and 53 respectively. This is presented in Figure 3.

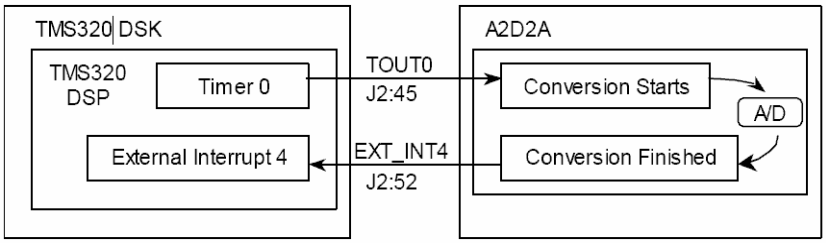

Figure 3
A/D Conversion Timing Control

The assumption presented on the timing diagram is that the appropriate supporting software is running on the DSP; hence, optimal A2D2A card usage is achieved. As presented in Figure 6, the TOUT0 pulse initiates the A/D conversion and it also starts a direct memory access (DMA) that updates the D/A converter's registers. These processes occur simultaneously. The four D/A registers are updated within 1.2 μs of the starting pulse. The A/D converter is designed to concurrently sample the eight channels within a few nanoseconds, thereby preserving the relative phase information between the input signals. At the end of A/D conversion, the E_INT4 interrupt signal initiates a second DMA access to the A2D2A card, in order to read the eight A/D registers. When the data transfer is complete, the DSP receives the INT8 interrupt, which signals that the converted data is ready for processing. In this design, the maximum conversion frequency can be selected as 83 kHz.

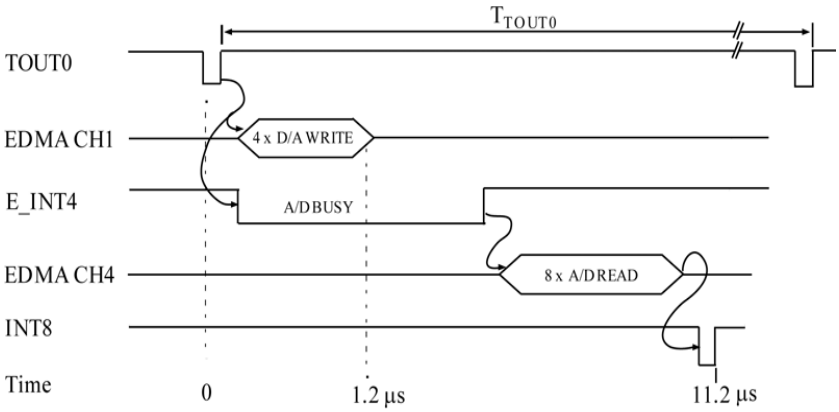

Figure 4
Timing Diagram for A2D2A

3 Enhancement of A/D Conversion

In the implemented scenario, the A/D and D/A converters are utilized to convert specifically at the frequency of 50.0 kHz, which corresponds to 20 μs TTOUT0 period. The DSP collects from all the eight channels sixteen samples of consecutive A/D conversion data and after calculating the average of the A/D conversions, it makes the data available every 0.32 ms to the rest of the processes. The data flow, for this implementation, is presented on Figure 5. The filter on the measured data is further analyzed in the following.

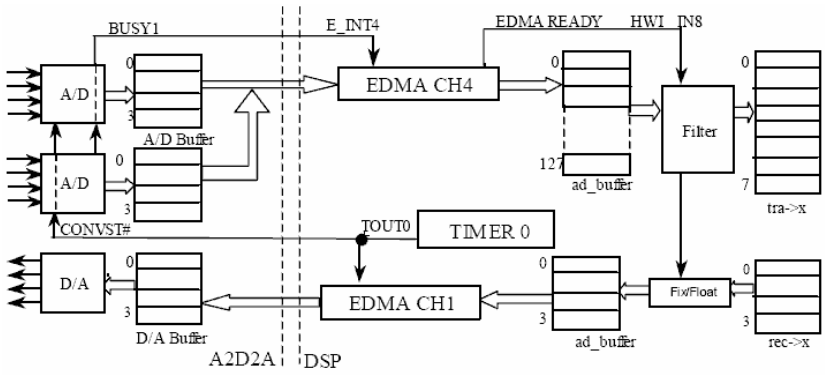

Figure 5
Data flow between A2D2A and the DSP

4 Programming the PLD

All the necessary control functions of the A2D2A are implemented in a Programmable Logic Device (PLD). The communication between the TMS320 DSK and the A2D2A card is facilitated by both the Memory Connector (J1) and Peripheral Connector (J2).

4.1 Chip Select

The access to the A2D2A registers is enabled if the chip select line J1:78, DC_CSa# is at a low level [1]. This chip select line on the Memory Connector's 78 pin is recognized by the DSP as either: CE2, CE1, DS# or XCE0# depending on which EVM or DSK is used [1]. Specifically, the chip select line for the TMS320C6711DSK corresponds to CS2, which is activated if the DSP selects a memory space of 0xA0000000 and above.

The selected device for the control logic is an electronically configurable PLD, EMP7032AE, from Altera Corporation. The configuration is done through a JTAG interface when it is connected to the DSK, which powers both the PLD and the JTAG interface units, shown in Figure 6. The used JTAG interface with a parallel port connection to a personal computer is also constructed for this event following the instructions available at the Altera website [2]. For the configuration and the design a freely available software is used from the Altera website.

For the JTAG connection, to save space, no formal connector is designed rather test points are included, which are clearly marked in the upper cupper layer with TDO, TDI, TMS, GND, and 3.3V symbols. For the connection, five thin insulated wires are soldered to these points, which are removed after the configuration has been done.

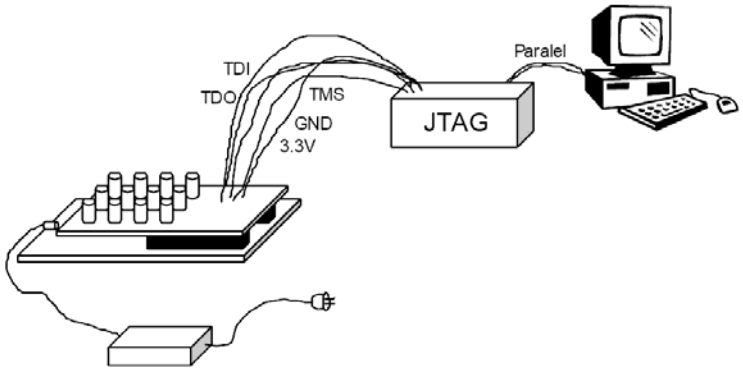

Figure 6
The A2D2A Configuration

Conclusions

Daughter cards similar to the system described here are also produced by Texas Instruments [3], for example, for sound processing. Another developer developed other for high-speed signal processing [4]. These devices have 1 or 2 in-and outputs and cannot be configured at will. The developing board described here in this article in detail enables digital signal processing at higher sampling speed, where more in- and outputs and greater resolution are needed. This developing board provides precise, multi-channel digital signal processing.

References

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