ANALOG INTERFACE CARD - A2D2A

For Texas Instruments DSP Development Systems

Hardware for Signal Processing & Control

AFFORDABLE HARDWARE IMPLEMENTATION

Hardware for Signal Processing and Control

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Abstract

Analog to Digital & Digital to Analog converter interface card – A2D2A

The design of an interface card with eight analog inputs and four analog outputs is described in this technical paper. The standards stipulated in Texas Instruments *TMS320 Cross-Platform Daughtercard Specification, Revision 1.0*, [1] have been followed in the design process. This card can be used with any Texas Instruments TI320 DSP development system, as presented in Figure 1. The A2D2A generates all of the necessary voltages on board from the 5V power, which is available according to the *TMS320 Cross-Platform Daughtercard Specifications*. For an easy interface, the common BNC coaxial connectors are used for the input and output connections. To reduce the manufacturing costs, the card is designed using a two layer PCB.

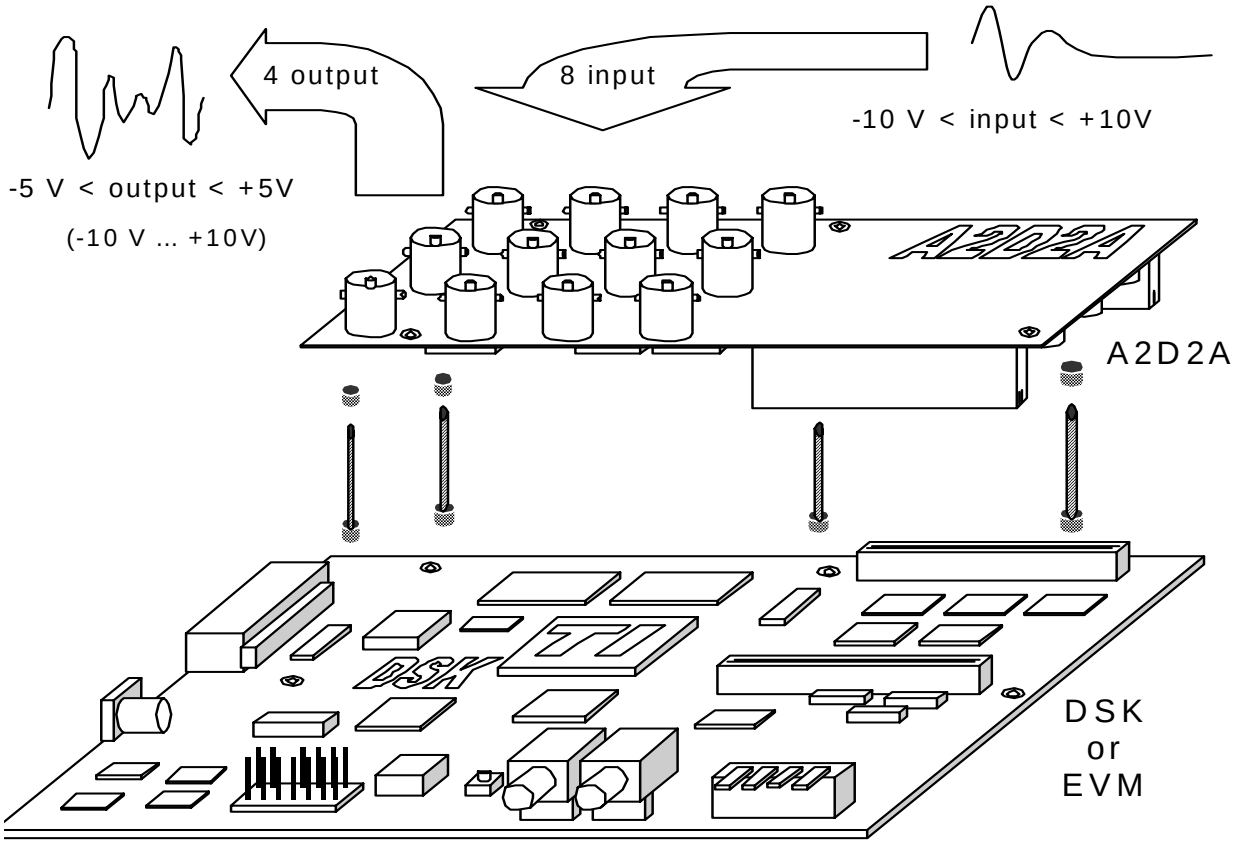

Figure 1 Usage of the A2D2A daughtercard

Table of Contents

Introduction

Signal processing and control algorithms have increased in complexity since their introduction in the 1960's. The main research tools that have contributed to the development of these algorithms are simulation tools such as matlab from The MathWorks. Although these tools have become increasingly sophisticated, the evaluation of the proposed algorithms can only be performed through real-time experiments.

The implementation of signal processing and control algorithms in real-time experiments has become more feasible with the introduction of Digital Signal Processors (DSP). For implementation, it is required that these DSPs be constructed in the form of embedded systems. On the market, more than one system is available with the ability to perform either general or specific functions. These systems are frequently characterized by high price and a low lifespan, due to their fast evolution. Fortunately, all the DSP manufacturers sell their DSPs in the form of a development system, consisting of a minimal hardware and a development software bundle at an affordable price. Although the supplied hardware enables real-time algorithm development, the required connection to the analog world is seldom included. In order to overcome this problem, the DSP development boards are equipped with expansion connectors which allow the attachment of daughtercards. Only a few companies, such as Analog Devices, Motorola, and Texas Instruments, dominate the market of DSPs.

In the following, the A2D2A interface card is described, which can be used by Texas Instruments development systems. This document is written not only with the intention to describe the developed A2D2A analog interface card but also with the objective is to present adequate information that aids the design of similar interface cards.

A2D2A Card

The top view of the A2D2A daughtercard is shown in Figure 2. The upper eight BNC connectors are the analog inputs while the lower four BNC connectors are the analog outputs. To prevent both mechanical and electrical damage to the card, the top surface does not contain electrical elements.

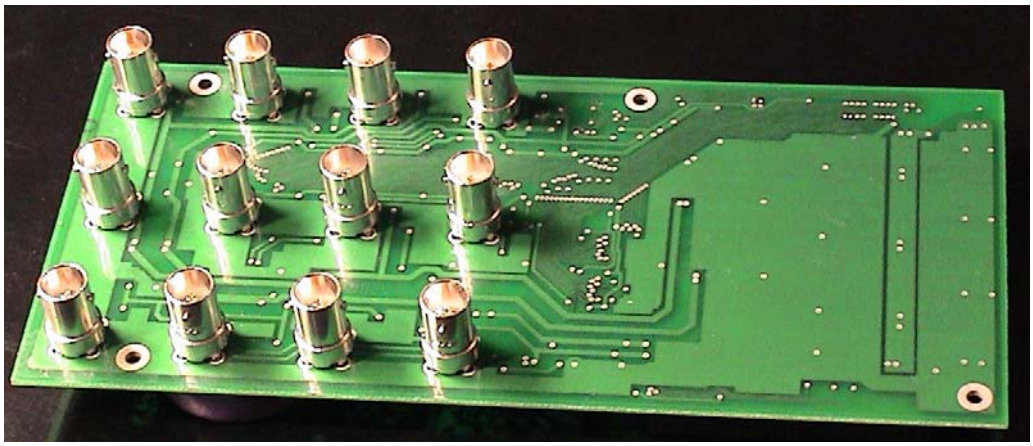

Figure 2 A2D2A: Top View

The electrical components are mounted on the bottom panel, as presented in Figure 3. The power converter section, located to the left, is between the two connectors. On the photo, the A/D section is to the upper right and the D/A section is to the lower right.

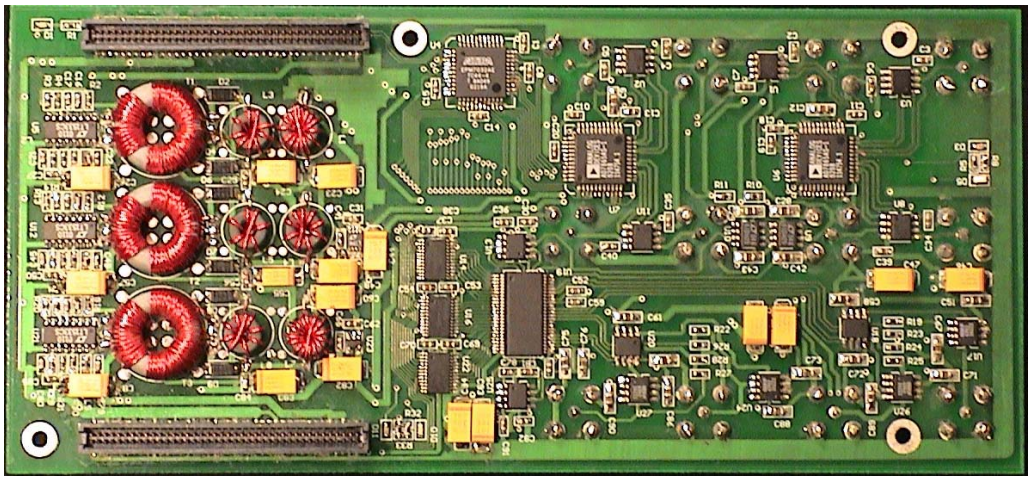

Figure 3 A2D2A: Bottom View

Highlights

The A2D2A interface card, which facilitates communication between a TMS320 DSP development system and the analog environment, contains eight analog to digital (A/D) converter channels and four digital to analog (D/A) converter channels. For easy interfacing, the card uses common BNC coaxial connectors. The characteristic components of the interface card are listed in Table 1, while its block diagram is presented in Figure 4.

The A2D2A card offers eight channels of 14-bit A/D conversions and a sampling rate which can attain a frequency of 83kHz, as well as four channels of 16-bit D/A conversions, making it ideal for data acquisition in multidimensional signal processing, transient capture, and control systems.

Any sampling rate from 0 Hz to 83 kHz can be derived from the internal clock of the DSP. Due to the employed A/D converter, AD7865AS-1, from Analog Devices, all channels are sampled simultaneously with virtually zero phase delay. Both the inputs and the outputs are equipped with appropriate amplifiers, which increase the input resistance and ensure the adequate output signal power.

Main Characteristics of the A2D2A Card

- **Input:** single-ended, ±10.0 V, full scale, 250 GΩ impedance
- **Output:** ± 5.0 V, full scale, low output impedance, up to ± 250 mA, thermal protection
- **A/D and D/A conversions:** 14-bit and 16-bit respectively
- **Sampling rate:** provided by an internal DSP clock, varies from 0 Hz to 83 kHz
- **Power:** 1.0 A at +5 V supplied by the DSP board

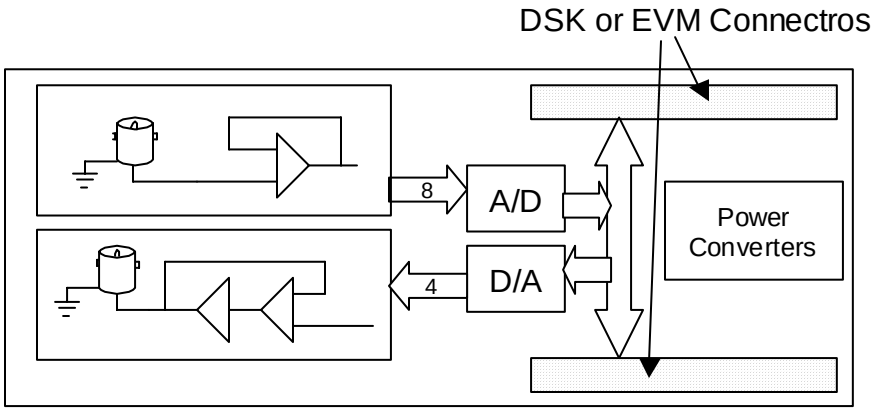

Figure 4 A2D2A: Block Representation

Table 1: Characteristic Components of the A2D2A Card

Description	Part Number	Quantity	Manufacturer
A/D Converter	AD7865AS-1	2	Analog Devices
D/A Converter	DAC7644E-ND	1	Burr-Brown
Voltage Reference	LT1461DHS8-2.5	2	Linear Technology
Operational Amplifier	OPA2277UA	9	Burr-Brown
Buffer	BUF634U	4	Burr-Brown
Switching Power Supply	LT1533CS	3	Linear Technology
3.3V to 5V Interface	SN74LVC4245APWR	3	Texas Instruments
Control Logic	EMP7032AE	1	Altera Corporation

In order to simplify the card's usage, the A2D2A is equipped with its own voltage converters of -12, -5, 5, and 12 V. These voltage converters are necessary for the board's functioning.

Description

One of the design objectives was to minimize the required interaction between the A2D2A card and the DSP. This was accomplished by the following manner. The timing of the A/D conversion is directly connected to the DSP's clock output. When the A/D conversion is complete, it generates an interrupt on the DSP. This is used to initiate a Direct Memory Access (DMA) transfer to read the converted data. At the end of the DMA transfer, a new interrupt is generated, which signals to the DSP that the A/D data is ready for processing. The D/A conversion control is further simplified when the write action automatically generates the D/A conversion. Next, the different units of the A2D2A card are described.

Timing Control

The timing of the A2D2A's conversion is initialized by a TOUT0 signal that is generated by the DSP's Timer 0. The resulting conversion lasts about 12μs. Following the completion of the conversion, an EXT_INT4 signal is generated. This signal is connected to the DSP's external interrupt line and generates an interrupt in the DSP, signaling that the data is ready for reading on the A2D2A card. The TOUT0 and the EXT_INT4 signals are the DSK's Peripheral Connector (J2) pins, 45 and 53 respectively. This is presented in Figure 5.

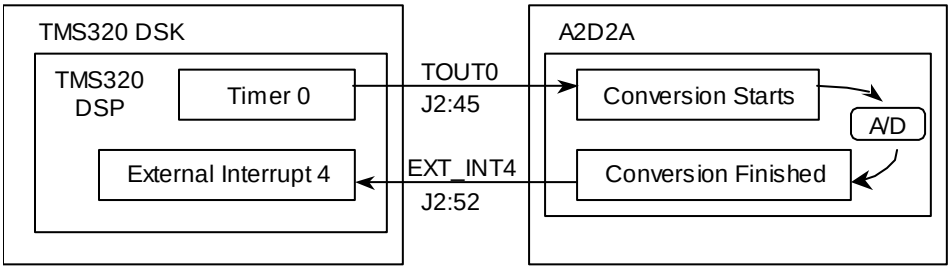

Figure 5 A/D Conversion Timing Control

Timing Diagram

The assumption presented on the timing diagram is that the appropriate supporting software is running on the DSP; hence, optimal A2D2A card usage is achieved. As presented in Figure 6, the TOUT0 pulse initiates the A/D conversion and it also starts a direct memory access (DMA) that updates the D/A converter's registers. These processes occur simultaneously. The four D/A registers are updated within 1.2 μs of the starting pulse. The A/D converter is designed to concurrently sample the eight channels within a few nanoseconds, thereby preserving the relative phase information between the input signals. At the end of A/D conversion, the E_INT4 interrupt signal initiates a second DMA access to the A2D2A card, in order to read the eight A/D registers. When the data transfer is complete, the DSP receives the INT8 interrupt, which signals that the converted data is ready for processing. In this design, the maximum conversion frequency can be selected as 83 kHz.

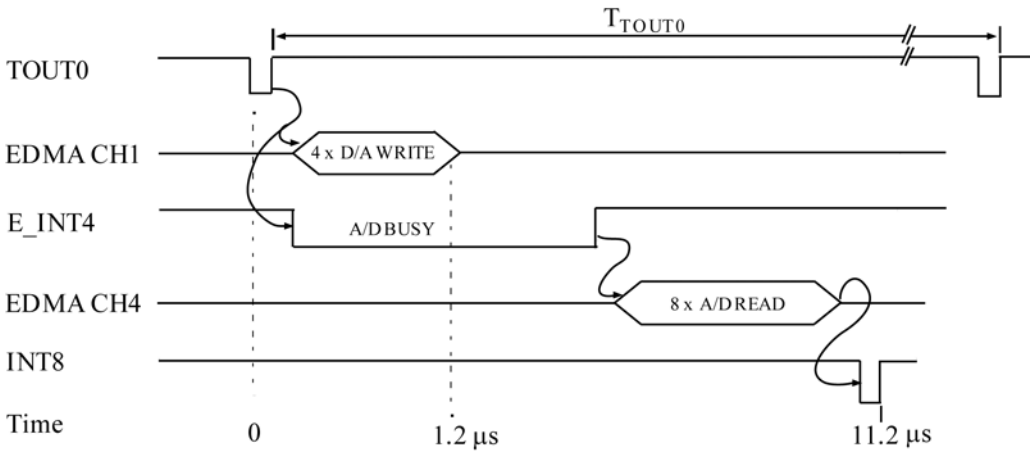

Figure 6 Timing Diagram for A2D2A

DSP and A2D2A Communication

A detailed connection diagram, presenting the used signals, is shown in Figure 7. All the necessary control functions of the A2D2A are implemented in a Programmable Logic Device (PLD). The communication between the TMS320 DSK and the A2D2A card is facilitated by both the Memory Connector (J1) and Peripheral Connector (J2).

Chip Select

The access to the A2D2A registers is enabled if the chip select line J1:78, DC_CSa# is at a low level [1]. This chip select line on the Memory Connector's 78 pin is recognized by the DSP as either: CE2, CE1, DS# or XCE0# depending on which EVM or DSK is used [1]. Specifically, the chip select line for the TMS320C6711DSK corresponds to CS2, which is activated if the DSP selects a memory space of 0xA0000000 and above.

Address Space

The address space of the A2D2A is only 16 words long, as presented in Table 2. The address lines are connected to the J1:26:23 pins of the DSP's Memory Connector.

Table 2: The Memory Space of the A2D2A Card

Address Space	Device	Access
0 - 3	Future Use	-

4 - 7	A/D Channels 1-4	Read
8 - 11	A/D Channels 5-8	Read
12 - 15	D/A Channels 1-4	Write

Specifically, the space for the TMS320C6711DSK is located at the addresses from 0xA0000000 to 0xA000003C, by the increment of 0x4. Thus, the A/D Channel 1 can be read on address 0xA0000010, Channel 2 on address 0xA0000014, and so on. The D/A Channel 1 can be written on address 0xA0000030, D/A Channel 2 on 0xA0000034, and so on.

Control Signals

The access to A2D2A card is controlled by signals ARE#, AWE# and AOE# on the J1:73, J1:74 and J1:75 pins, respectively. It is mandatory that the DSP's memory access timing is configured to satisfy the requirements stipulated in [2]and [3].

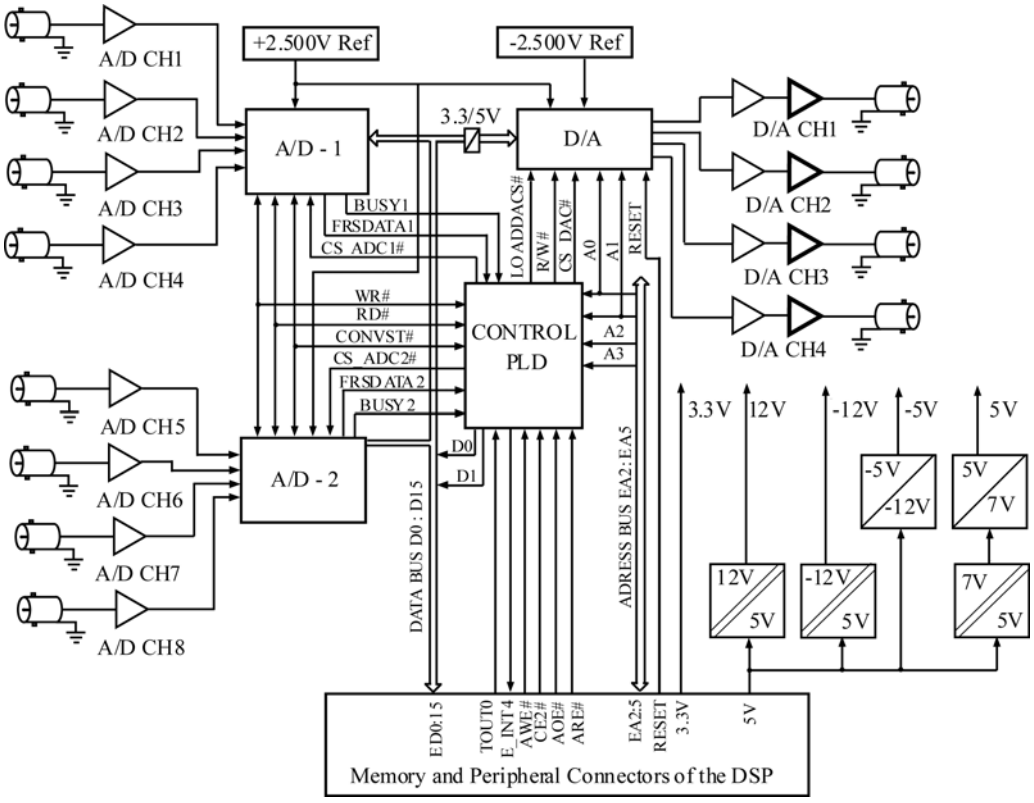

Figure 7 Connection Diagram of A2D2A

Input Buffer

In order to increase the input resistance a high precision operation amplifier, OPA2277 from Burr-Brown Corporation [4], is implemented. The OPA2277 is free from phase inversion and overload problems. It is stable in the implemented unity gain and provides excellent dynamic behavior.

The inputs of the A2D2A card are protected by the built in 1 kΩ series input resistors and diode clamps of the OPA2277. The inputs can withstand ±30 V differential inputs without damage. The protection diodes will, of course, conduct current when the inputs are over-driven. This may disturb the slewing behavior of the unity-gain follower application, but it will not damage the card [4].

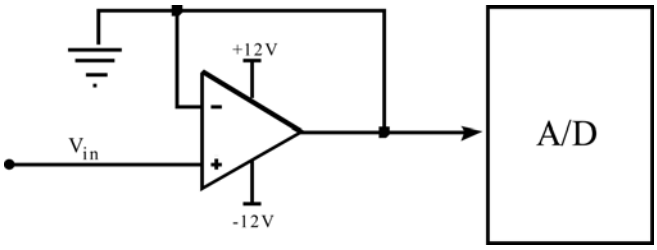

Figure 8 Input Signal Buffering

Output Buffer

The output is constructed by using a combination of an operation amplifier [4] and a high-speed buffer, BUF634, from Burr-Brown Corporation [5]. In this circuit configuration, as presented in Figure 9, the work is divided so that the operation amplifier is responsible for precision while the buffer provides the necessary current. An important advantage of this combination is that the power dissipation is managed by the buffer. The operation amplifier is loaded only by the low input current of the buffer. The circuit parameters such as offset, drift, noise, and harmonic distortion depend almost entirely upon the operation amplifier used in the circuit [6]. The output from the D/A converter is ± 2.5 V (full scale). For the selected R1 = R2 = 10.0 kΩ, the gain of the buffer becomes G = 1+(R2/R1) = 2 and the buffer's output is in the range of ± 5.0 V (full scale). The maximum gain, for the ± 2.5 V full scale input voltage with the ± 12 V power supply, is when G = 4. This can be obtained by selecting R2 = 30.0 kΩ from the standard 1% resistor group.

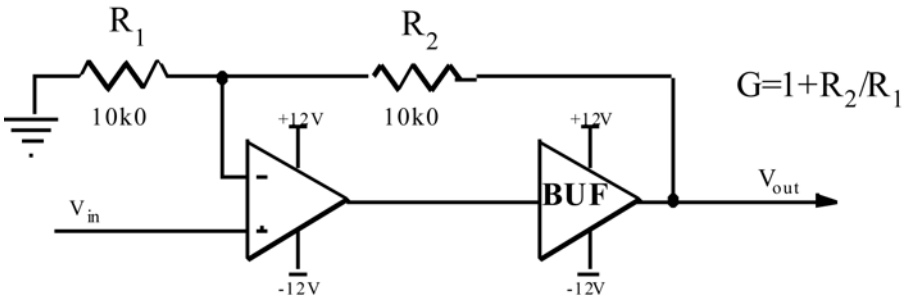

Figure 9 Output Signal Buffering

Reference voltages

Positive Reference

The A/D and D/A converters require reference voltages of + 2.500 V and -2.500 V. To attain the highest precision, the LT1461 from Linear Technology has been selected [7]. The LT1461 combines very high accuracy and low drift with low supply current requirements. The design of the + 2.500V reference on the A2D2A card follows the recommendations from [7], as presented in Figure 10.

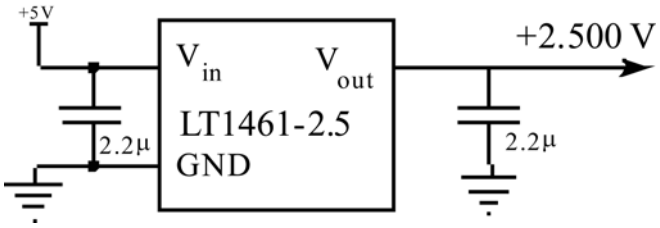

Figure 10 Positive Reference

Negative Reference

In order to obtain a high accuracy negative reference, the LT1461 is used in a modified connection, Figure 11. Although LT1461 is used as very stable negative reference, it requires a positive voltage applied to the Vin to bias internal circuitry. The input positive voltage must be current limited with a resistor to keep the output PNP transistor from turning on and driving the grounded output, Vout. The -2.500 V reference design is presented in Figure 11.

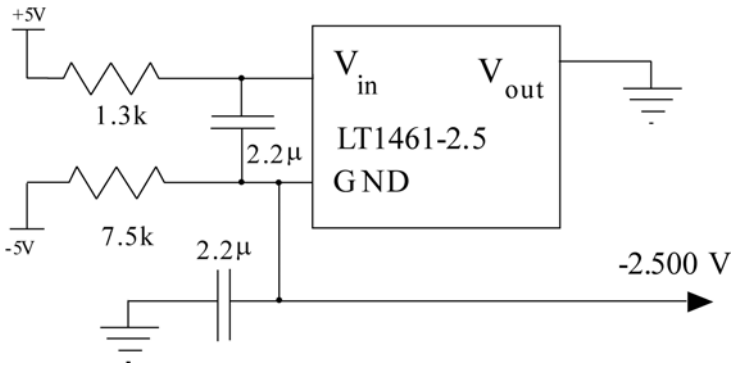

Figure 11 Negative Reference

Interpretation

The connection between the real word of the input/output voltages and the corresponding representation of this in the DSP is available in Table 3 and Table 4.

Table 3: A/D Conversion Characteristics

Voltage on the Input	Raw Count Read	Float Representation
- 10 V	0x8000	-10.0
0 V	0x0000	0.0
+ 10 V	0x7FFF	10.0

Table 4: D/A Conversion Characteristics

Voltage on the Output	Raw Count	Float Representation
- 5 V	0x0000	-5.0
0 V	0x8000	0.0
+5 V	0xFFFF	5.0

Shielding

During the initial tests it was observed that the proximity of the DSP and the A/D converters resulted in a noisier measurement than it is normally expected. After some experimentation a shielding was designed between the DSP and the A2D2A card, as presented in Figure 1. The shield is made of a thin sheet of tin according to the specifications given in Figure 13. The shield considerably reduces the noise on the measured data.

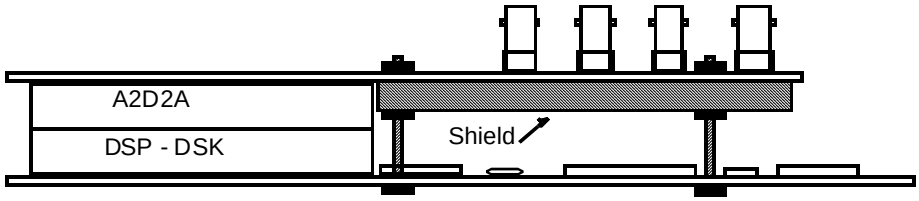

Figure 12 The Mounted Shield

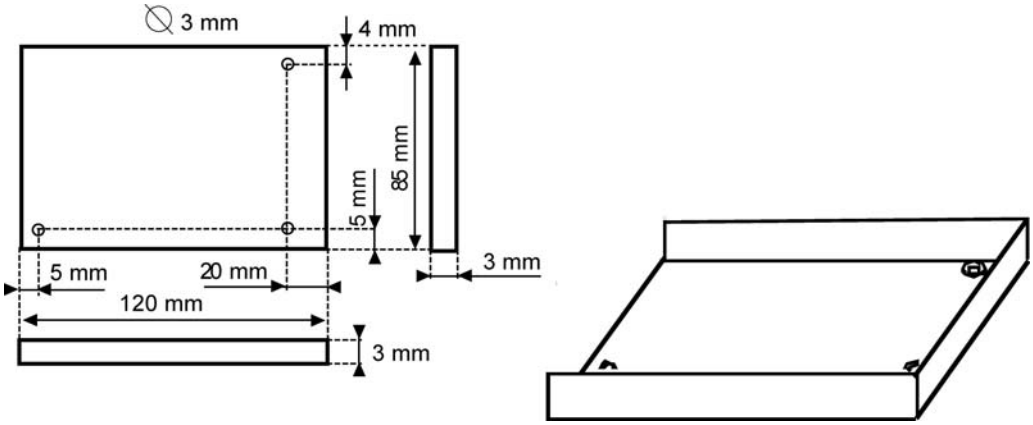

Figure 13 Shield Specifications

Power Source

The DSP connectors only provide 3.3V power for the digital signal drivers and 5V with maximum 1.0 A electric power for the daughtercard powering. The components on the A2D2A card require -12V, -5V, 5V and 12V. Using external power sources would be expensive and it could also introduce more possibility for error. The simplest and safest approach is to generate the required powers on board, using DC/DC

converters. For this reason, three DC/DC switching power converters were added to the A2D2A card, to convert the 5V input power to -12V, 7V and 12V. Further, linear regulators are used to produce the -5V from -12V and 5V from 7V. The linear regulators ensure that the noise on the power is even less than that on the already low noise switching DC/DC converters.

The most important component of the DC/DC converter is an ultra low-noise switching regulator, the LT1533CS from Linear Technology [7]. This controller is considered as the least noisy switching power supply on the market. For the design the suggested schema from Linear Technology is used with one modification. Since the suggested transformers were not available in small quantities, these were replaced with transformers made from toroid cores from Magnetics[1] and manual winding. For the transformers the ZR-41605-TC core is selected. The inductive filters are using the OW-40705-TC cores.

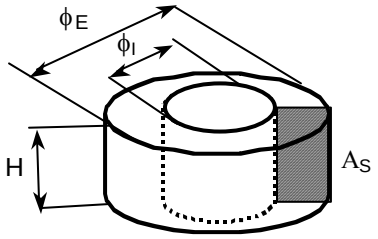

Figure 14 Dimension Definitions

ZR-41605-TC: ϕ_E=15.9*mm*, ϕ_I=8.89*mm*, H=4.7*mm*, A_S=0.153cm^2, AL= 1.260 *mH/turns*

OW-40705-TC: ϕ_E=7.6*mm*, ϕ_I=3.18 *mm*, H=4.7*mm*, A_S=0.-98cm^2, AL = 8.350 *mH/turns*

ϕ_E is the external diameter, ϕ_I is the internal diameter, H is the height of the ferrite toroid core and AL is the magnetic field generated by a single turn.

The required number of turns is determined by the Faraday's law [12]:

$$N_P = \frac{(V_{in} - V_F) \cdot \left(0.8 \cdot \frac{1}{2 \cdot f_{SW}} \right) \cdot 10^8}{A_S \cdot \Phi} \qquad \text{Eq 1}$$

where :

V_{in} = 5V is the input DC voltage

[1] Magnetics Division of Spang & Company

V_F= 1V is the forward voltage drop of the rectifier

f_{SW}= 90 kHz is the selected switching frequency of the push-pull converter

A_S= 0.153 cm^2 effective cross section area of the core

Φ_p= 1000G = 0.1T peak flux density.

The number of primary turns is inversely proportional to peak flux density, Φ_p. In order to minimize the required number of turns, N_p, it would seem desirable to maximize Φ_p. Above 50 kHz, increasing core losses forces a decrease in peak flux density. At 100 to 200 kHz, the peak flux density may have to be limited to 1200 or possibly to 800 G, respectively, to achieve an acceptable low core temperature rise [12].

The calculated required primary turns are $N_p = 11.62 \rightarrow 12$.

The secondary turns number is calculated through the secondary to primary turns ratio N_s / N_p equations [7]

$$N_S / N_p = \frac{V_{out} + V_F}{2 \cdot T_d \cdot \left(V_{in\min} - V_s\right)} \qquad \text{Eq 2}$$

where V_{out} = 12V and V_{out} = 7V, for the desired output voltages of +/-12V and 7V respectively.

V_F = 0.5 forward drop of the rectifier [7]

T_d = 0.44 the maximum duty cycle of each driver. For the LT1333 it is 0.44 [7]

V_{inmin} = 4.5V the expected minimum input voltage

V_s = 0.5V_F = 0.5 switch on voltage [7].

The resulting ratio of the secondary to primary turns is N_s / N_p = 44 and N_s / N_p = 27 for +/-12V and 7V respectively.

The detailed winding is presented in Figure 15. The connection of the transformer is presented in Figure 16.

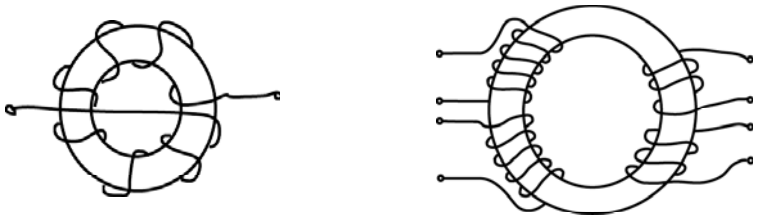

Figure 15 Inductor / Transformer winding

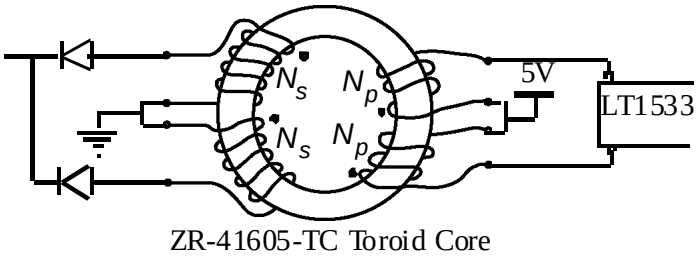

Figure 16 Transformer connection

The power supply section of the A2D2A is presented in picture Figure 17, where the three transformers with six inductor-filters can be clearly observed between the Peripheral and Memory connectors.

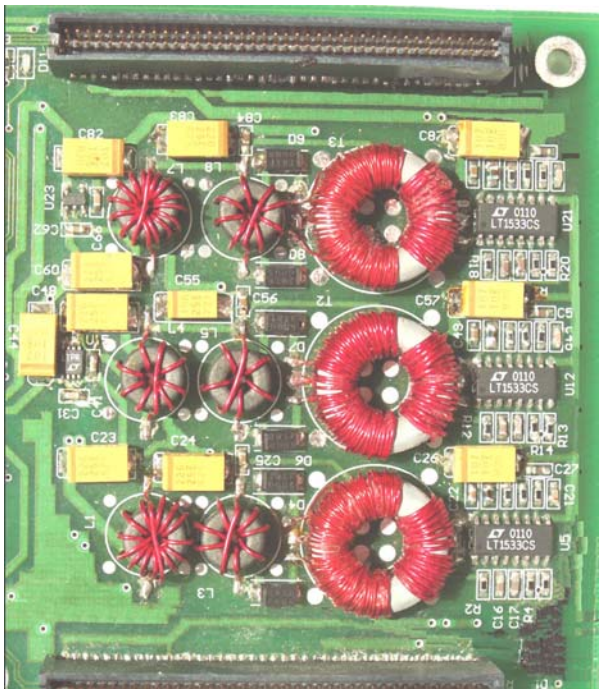

Figure 17 The Realized Power Section

Enhancement of A/D Conversion

In the implemented scenario, the A/D and D/A converters are utilized to convert specifically at the frequency of 50.0 kHz, which corresponds to 20 μs T_{TOUT0} period. The DSP collects from all the eight channels sixteen samples of consecutive A/D conversion data and after calculating the average of the A/D conversions, it makes the data available every 0.32 ms to the rest of the processes. The data flow, for this implementation, is presented on Figure 18. The filter on the measured data is further analyzed in the following.

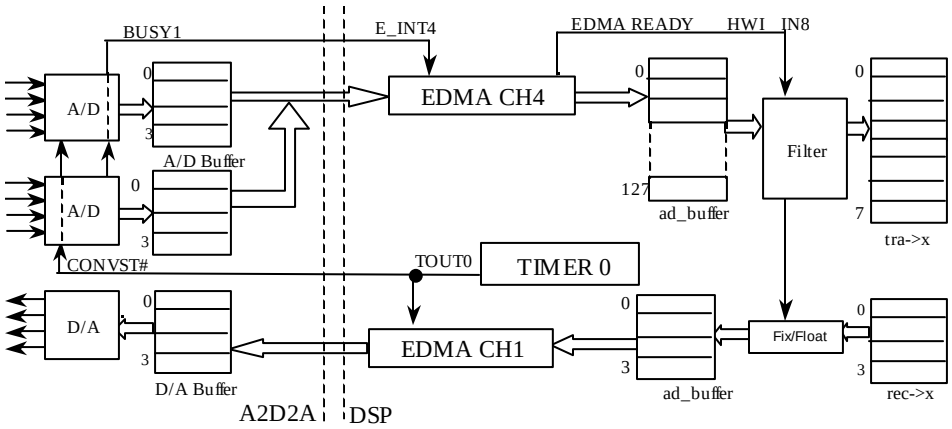

Figure 18 Data flow between A2D2A and the DSP

In general, the data y_n from the A/D conversion contains some error due to the effects of the conversion process and the necessary signal conditioning prior to it. Usually this error can be modeled by an additive random signal ξ_n, superposed on the measured signal y_n^0 [8]

$$y_n = y_n^0 + \xi_n \qquad \text{Eq 3}$$

The accuracy of the A/D conversion improves if the signal to noise ratio is increased in the measurement. This is attained if multiple A/D conversions are performed and an average is calculated

$$\overline{y_n} = \tfrac{1}{N} \cdot \sum_{i=0}^{N} y_{n-1} \ . \qquad \text{Eq 4}$$

For this procedure to be legitimate, the changes in the measured signal must be negligible on the length of the N sampling interval. Thus, $\bar{y}_n^0 \cong \bar{y}_{n-1}^0 \ldots \cong \bar{y}_{n-N}^0$ and

$$\bar{y}_n = \bar{y}_n^0 + \tfrac{1}{N} \cdot \sum_{i=1}^{N} \xi_{n-1} \qquad \text{Eq 5}$$

where $\bar{y}_n^0$ is the average of the measured signal. The increase in the signal to noise ratio by the averaging process depends on the distribution of this random signal ξ_n. In a technical environment, this signal is usually a normally distributed random signal (white Gaussian noise) with zero mean. In the worst case scenario, this signal can be a uniformly distributed random signal. It is important to stress that if the mean of the random signal ξ_n is other than zero, the averaging process will not improve the measurements; rather, it will emphasize the bias of the nonzero mean.

When the random signal $\xi_n \sim N(0, \sigma^2)$ is normally distributed with zero mean and variance σ^2, then the noise reduction in the A/D conversion data, obtained by averaging, is [9]

$$\bar{\xi}_n = \frac{1}{N} \sum_{i=1}^{N} \xi_{n-1} \ \text{ where } \xi_n \sim N\left(0, \tfrac{1}{N}\sigma^2\right) \qquad \text{Eq 6}$$

Even though the averaged signal is also normally distributed with a zero mean, there is a $1/N$ reduction in the noise variance, which corresponds to a $\sqrt{1/N}$ reduction of the standard deviation of the random signal. Consequently, the calculated average of 16 converted samples will improve the measurement accuracy by reducing four times the Gaussian noise in the measured data. In this way, the measurement accuracy improves by an extra two least significant valid bits.

When the random signal $\xi_n \sim U(-\omega, \omega)$ is uniformly distributed in the interval $-\omega \le \xi_n \le \omega$, the corresponding variance is $\sigma^2 = \omega^2 / 3$ [10]. It is well known that the distribution of the sum of N uniformly distributed random signals rapidly approaches normal distribution, as increases [11]. Accordingly,

$$\bar{\xi}_n = \frac{1}{N} \sum_{i=1}^{N} \xi_{n-1} \ \text{ where } \bar{\xi}_n \sim N\left(0, \tfrac{1}{N}\left(N \cdot \sigma^2\right)\right) \qquad \text{Eq 7}$$

The variance of the sum is linearly increasing by the number of summing elements. This means that if the random signal $\xi_n \sim U(-\omega, \omega)$ is uniformly distributed, the signal accuracy cannot be improved by the averaging process. Fortunately, very few technical systems have uniformly distributed contaminating signals.

Programming the PLD

The selected device for the control logic is an electronically configurable PLD, EMP7032AE, from Altera Corporation. The configuration is done through a JTAG interface when it is connected to the DSK, which powers both the PLD and the JTAG interface units, shown in Figure 19. The used JTAG interface with a parallel port connection to a personal computer is also constructed for this event following the instructions available at the Altera website. For the configuration and the design a freely available software is used from the Altera website.

For the JTAG connection, to save space, no formal connector is designed rather test points are included, which are clearly marked in the upper cupper layer with TDO, TDI, TMS, GND, and 3.3V symbols. For the connection, five thin insulated wires are soldered to these points, which are removed after the configuration has been done.

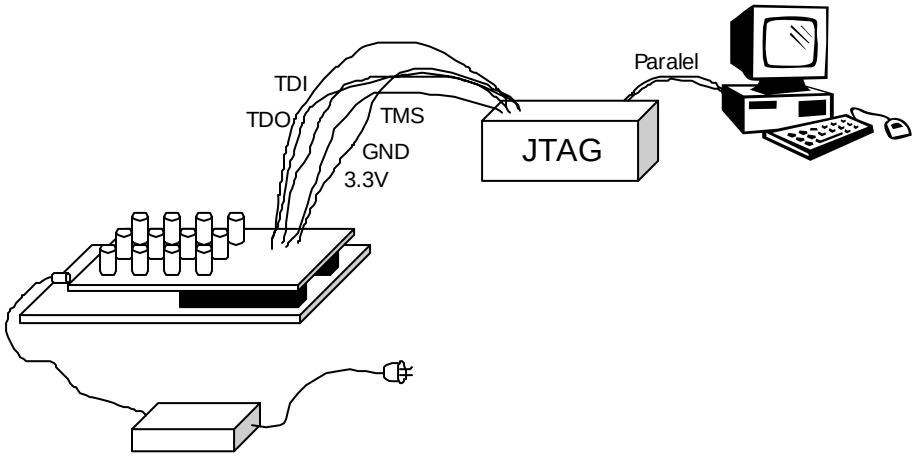

Figure 19 The A2D2A Configuration

References

[1] Bell, D., "TMS320 Cross-Platform Daughtercard Specification", Texas Instruments, Application Report, SPRA711, November, 2000.

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[3] Datasheet, "DAC7644 16-Bit, Quad Voltage Output Digital-to-Analog Converter", Burr-Brown Corporation, Tucson, AZ, USA, 1999.

[4] Datasheet, "High Precision Operational Amplifiers - OPA2277", Burr-Brown Corporation, Tucson, AZ, USA, 1999.

[5] Datasheet, "250mA High-Speed Buffer - BUF634", Burr-Brown Corporation, Tucson, AZ, USA, 1996.

[6] Vöhringer, U., "Combining an Amplifier with the BUF634", Burr-Brown International GmbH, Application Bulletin AB-101, Tucson, AZ, USA, 2000.

[7] Datasheet, "Micropower Precision Low Dropout Series Voltage Reference Family - LT1461", Linear Technology Corporation, Milpitas, CA, USA, 1999.

[8] Kay, S. M., "Fundamentals of Statistical Signal Processing, Volume 1: Estimation Theory", Prentice Hall - Signal Processing Series, NJ, USA, 1993.

[9] Papoulis, A., and Pillai, S. U., "Probability, Random Variables, and Stochastic Processes", Fourth Edition, McGraw-Hill, New York, NY, USA, 2002.

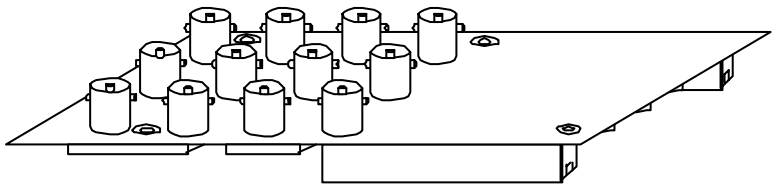
[10] Cramér, H., "Mathematical Methods of Statistics", Princeton University Press, Princeton, NJ, USA, 1958.

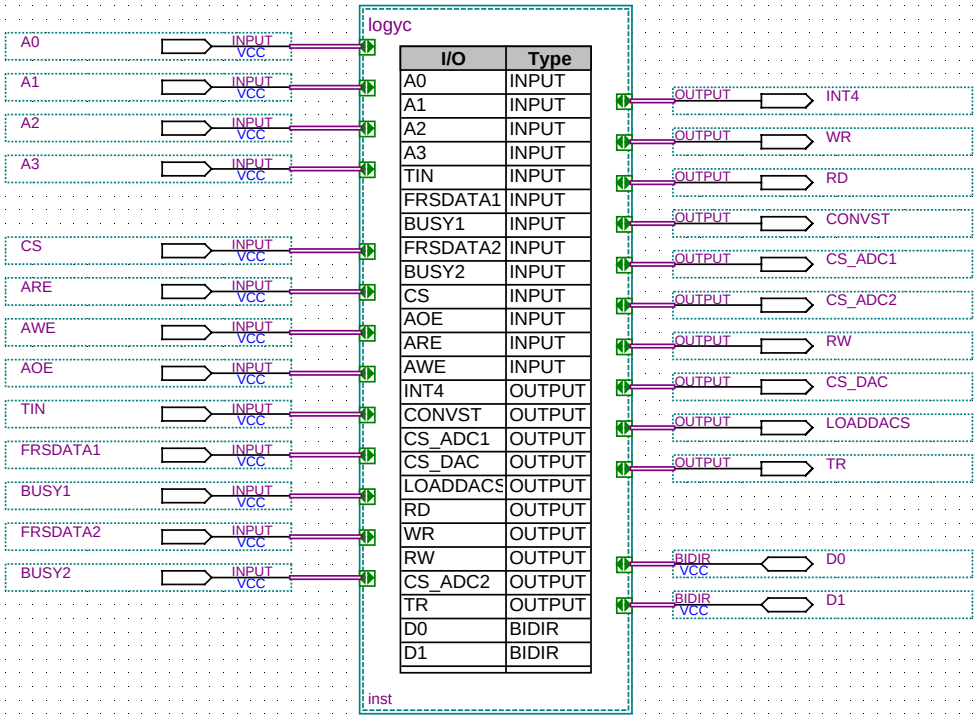
[11] Mitra, S. K., "On the Probability Distribution of the Sum of Uniformly Distributed Random Variables", SIAM Journal on Applied Mathematics, Vol. 20, No. 2, March, 1971, pp. 195-198.

[12] Pressman, I. A., "Switching Power Supply Design", McGraw-Hill, New York, NY, USA, 1997.

A2D2A Attached Documents

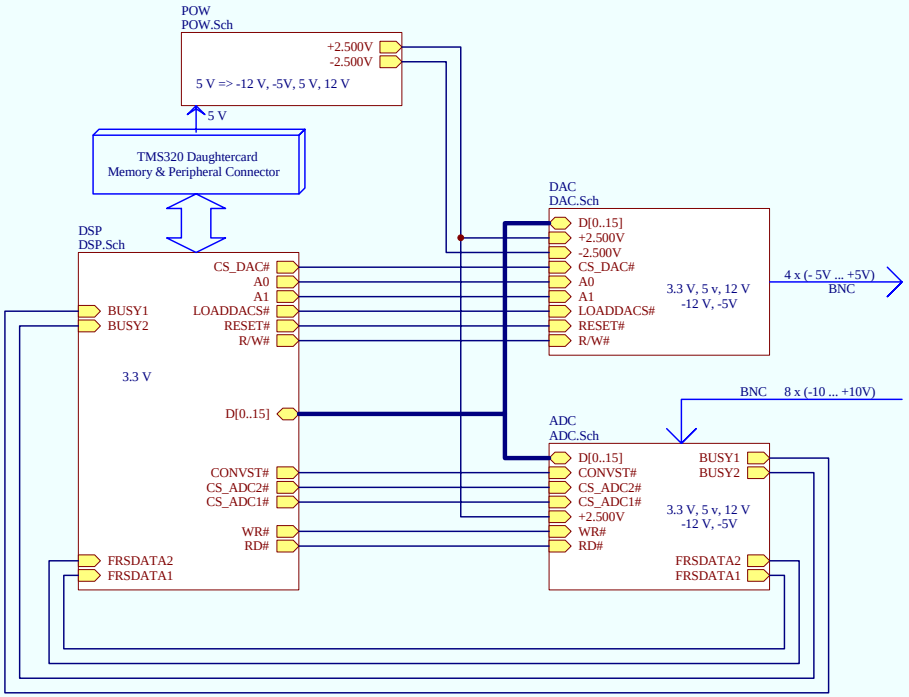
- **PLD Configuration Definition**
  - Input/Output signal interpretation of the PLD
  - VHDL code of the PLD
- **A2D2A Schematics**
  - Schematics Connection Block
  - Schematics 1/4
  - Schematics 2/4
  - Schematics 3/4
  - Schematics 4/4
- **PCB Image**
  - Top PCB layer
  - Bottom PCB layer




logyc
A0
A1
A2
A3
CS
ARE
AWE
AOE
TIN
FRSDATA1
BUSY1
FRSDATA2
BUSY2
INPUT
VCC
I/O
Type
A0 INPUT
A1 INPUT
A2 INPUT
A3 INPUT
TIN INPUT
FRSDATA1 INPUT
BUSY1 INPUT
FRSDATA2 INPUT
BUSY2 INPUT
CS INPUT
AOE INPUT
ARE INPUT
AWE INPUT
INT4 OUTPUT
CONVST OUTPUT
CS_ADC1 OUTPUT
CS_DAC OUTPUT
LOADDACS OUTPUT
RD OUTPUT
WR OUTPUT
RW OUTPUT
CS_ADC2 OUTPUT
TR OUTPUT
D0 BIDIR
D1 BIDIR
OUTPUT
INT4
WR
RD
CONVST
CS_ADC1
CS_ADC2
RW
CS_DAC
LOADDACS
TR
BIDIR
D0
D1
inst

```
1  -- Generated by Quartus II Version 2.2 (Build Build 147 12/02/2002)
2  -- Created on Wed Apr 02 02:42:20 2003
3
4  LIBRARY ieee;
5  USE ieee.std_logic_1164.all;
6
7  --  Entity Declaration
8
9  ENTITY logyc IS
10     -- {{ALTERA_IO_BEGIN}} DO NOT REMOVE THIS LINE!
11     PORT
12     (
13         A0 : IN STD_LOGIC;
14         A1 : IN STD_LOGIC;
15         A2 : IN STD_LOGIC;
16         A3 : IN STD_LOGIC;
17         TIN : IN STD_LOGIC;
18         FRSDATA1 : IN STD_LOGIC;
19         BUSY1 : IN STD_LOGIC;
20         FRSDATA2 : IN STD_LOGIC;
21         BUSY2 : IN STD_LOGIC;
22         CS : IN STD_LOGIC;
23         AOE : IN STD_LOGIC;
24         ARE : IN STD_LOGIC;
25         AWE : IN STD_LOGIC;
26         INT4 : OUT STD_LOGIC;
27         CONVST : OUT STD_LOGIC;
28         CS_ADC1 : OUT STD_LOGIC;
29         CS_DAC : OUT STD_LOGIC;
30         LOADDACS : OUT STD_LOGIC;
31         RD : OUT STD_LOGIC;
32         WR : OUT STD_LOGIC;
33         RW : OUT STD_LOGIC;
34         CS_ADC2 : OUT STD_LOGIC;
35         TR : OUT STD_LOGIC;
36         D0 : INOUT STD_LOGIC;
37         D1 : INOUT STD_LOGIC
38     );
39     -- {{ALTERA_IO_END}} DO NOT REMOVE THIS LINE!
40
41 END logyc;
42
43 --  Architecture Body
44
45 ARCHITECTURE logyc_architecture OF logyc IS
46
47 BEGIN
48
49     INT4 <= not ( BUSY1 or BUSY2);
50     CONVST <= TIN ;
51     CS_ADC1 <= CS or A3 or not A2 ;
52     CS_ADC2 <= CS or not A3 or A2 ;
53     CS_DAC <= CS or not A3 or not A2 or (ARE and AWE);
54     TR <= AOE;
55     LOADDACS <= CS or not A3 or not A2;
56     RW <= not AOE;
57     WR <= AWE;
```

```
58      RD <= ARE;
59
60      D0 <=   FRSDATA1 when (CS or A3 or not A2 or AOE) = '0'  else
61              FRSDATA2 when (CS or not A3 or A2 or AOE) = '0'  else
62              'Z';
63      D1 <= A1 when (CS or A3 or not A2 or AOE) = '0'  else
64             A1 when (CS or not A3 or A2 or AOE) = '0'  else
65              'Z';
66
67  END logyc_architecture;
68
```



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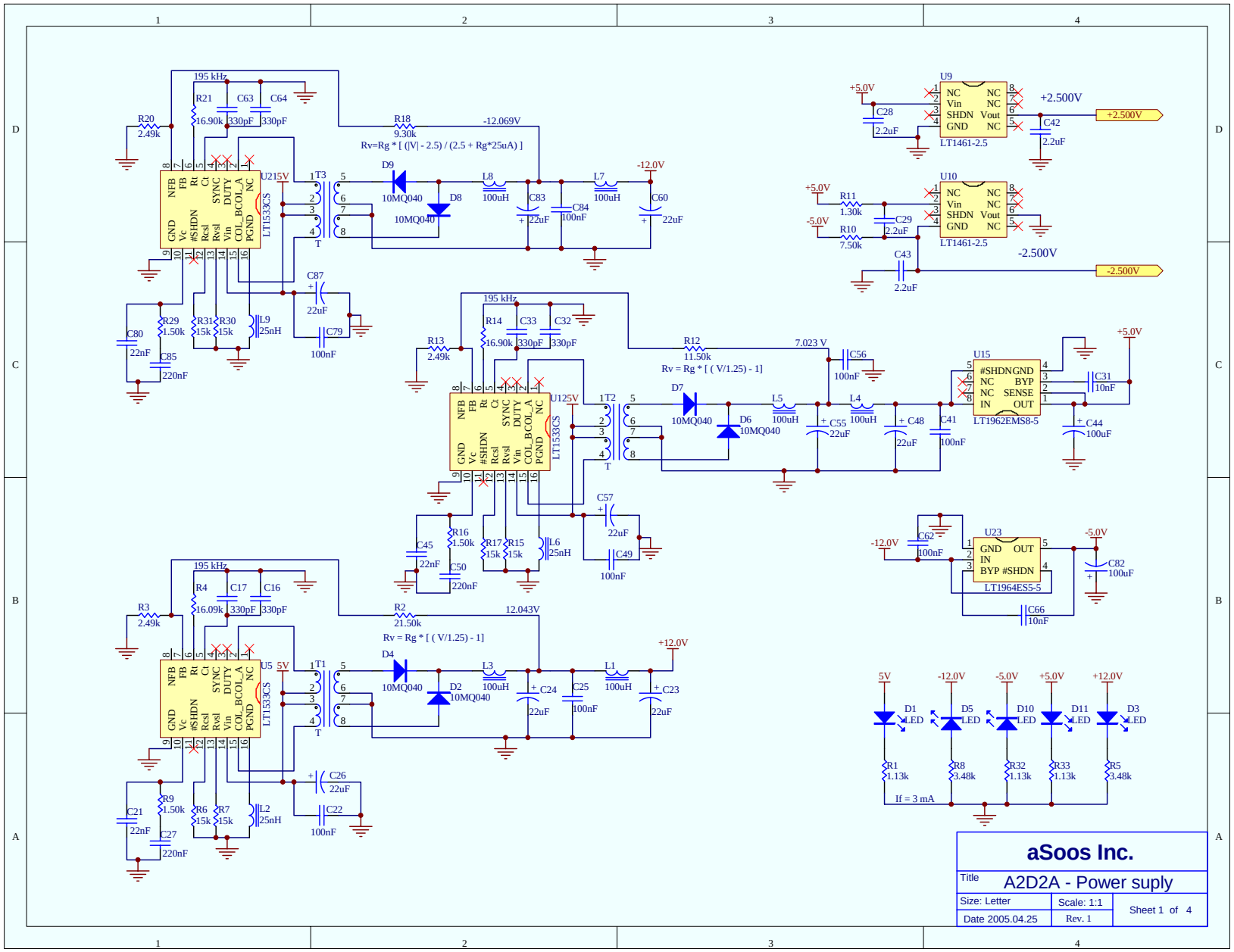
Date 2005.04.25	Rev. 1	


195 kHz
R21 16.90k
C63 330pF
C64 330pF
R20 2.49k
R18 9.30k
-12.069V
Rv=Rg * [(|V| - 2.5) / (2.5 + Rg*25uA)]
U2 15V
LT1533CS
NFB FB Rt Ct SYNC DUTY COL_BCOL_A NC
GND Vc #SHDN Rcsl Rvsl Vin PGND
T3
D9 10MQ040
D8 10MQ040
L8 100uH
L7 100uH
C83 22uF
C84 100nF
C60 22uF
-12.0V
C87 22uF
C79 100nF
R29 1.50k
R31 15k
R30 15k
L9 25nH
C80 22nF
C85 220nF
U9
NC NC Vin NC SHDN Vout GND NC
LT1461-2.5
+5.0V
C28 2.2uF
C42 2.2uF
+2.500V
U10
R11 1.30k
R10 7.50k
C29 2.2uF
C43 2.2uF
-5.0V
-2.500V
195 kHz
R14 16.90k
C33 330pF
C32 330pF
R13 2.49k
R12 11.50k
7.023 V
Rv = Rg * [(V/1.25) - 1]
U1 25V
T2
D7 10MQ040
D6 10MQ040
L5 100uH
L4 100uH
C56 100nF
C55 22uF
C48 22uF
C41 100nF
U15
#SHDN GND NC BYP NC SENSE IN OUT
LT1962EMS8-5
C31 10nF
C44 100uF
C57 22uF
C49 100nF
R16 1.50k
R17 15k
R15 15k
L6 25nH
C45 22nF
C50 220nF
U23
GND OUT IN BYP #SHDN
LT1964ES5-5
C62 100nF
C82 100uF
C66 10nF
195 kHz
R4 16.09k
C17 330pF
C16 330pF
R3 2.49k
R2 21.50k
12.043V
Rv = Rg * [(V/1.25) - 1]
U5 5V
T1
D4 10MQ040
D2 10MQ040
L3 100uH
L1 100uH
C24 22uF
C25 100nF
C23 22uF
+12.0V
C26 22uF
C22 100nF
R9 1.50k
R6 15k
R7 15k
L2 25nH
C21 22nF
C27 220nF
5V
D1 LED
D5 LED
D10 LED
D11 LED
D3 LED
R1 1.13k
R8 3.48k
R32 1.13k
R33 1.13k
R5 3.48k
If = 3 mA
aSoos Inc.
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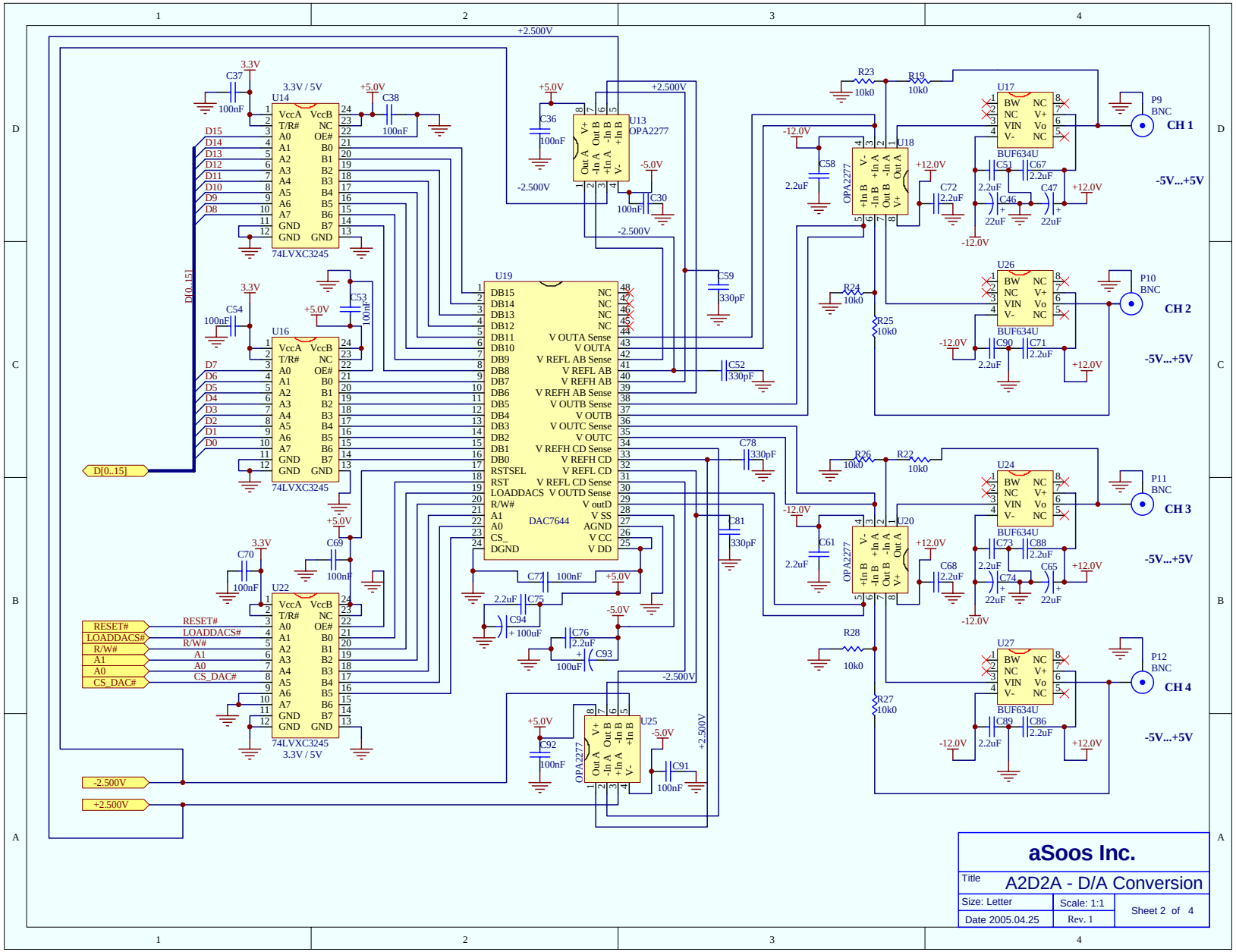
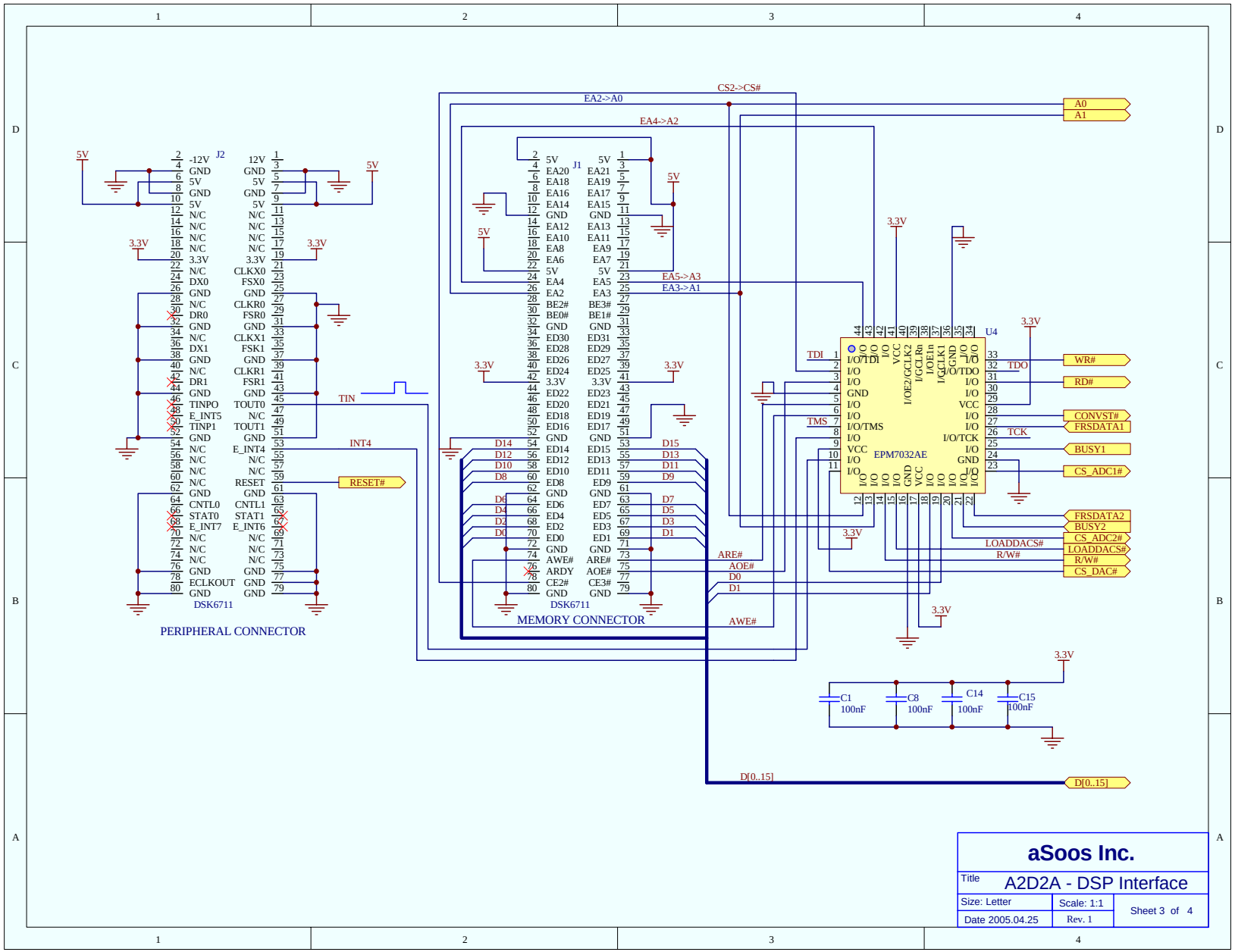
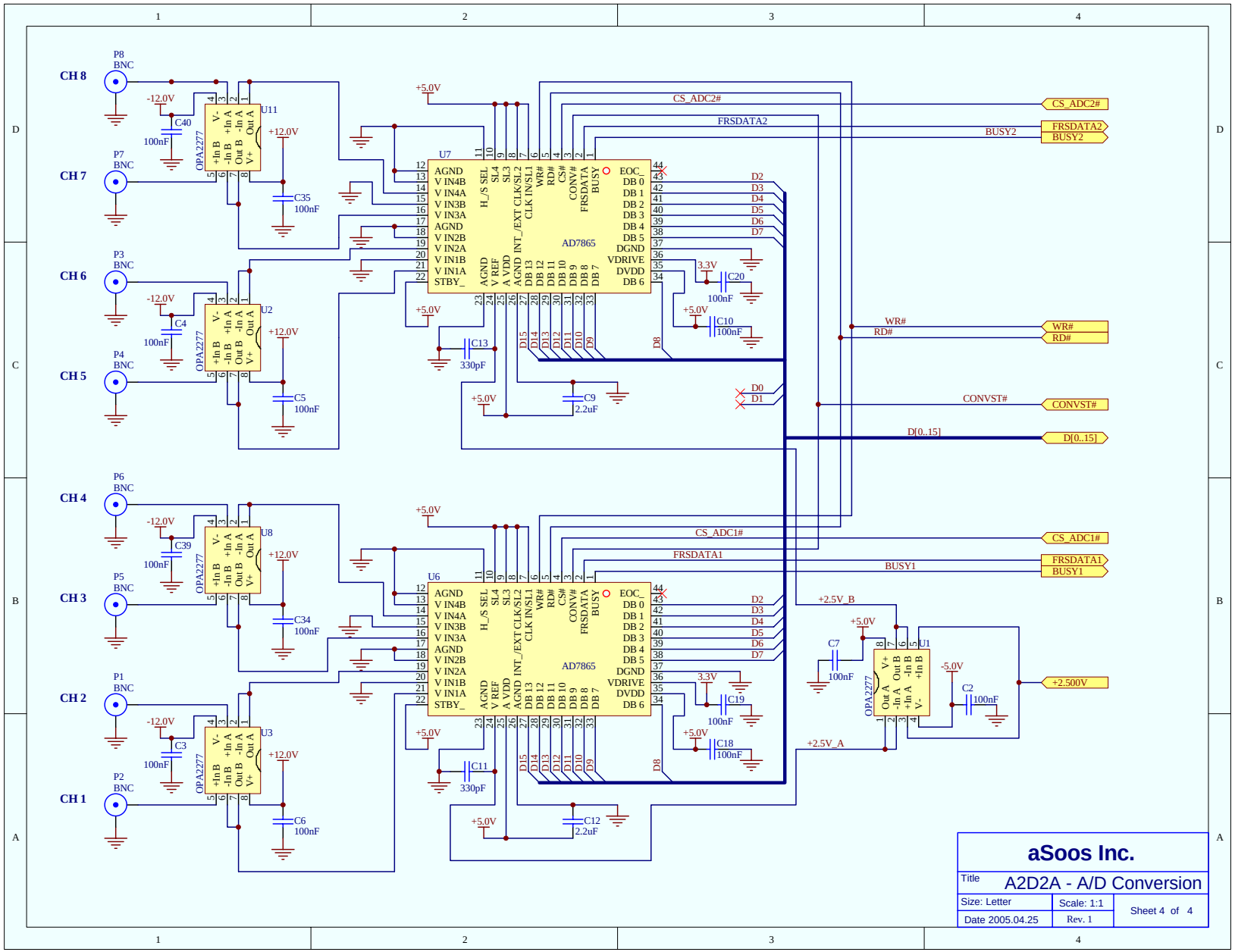
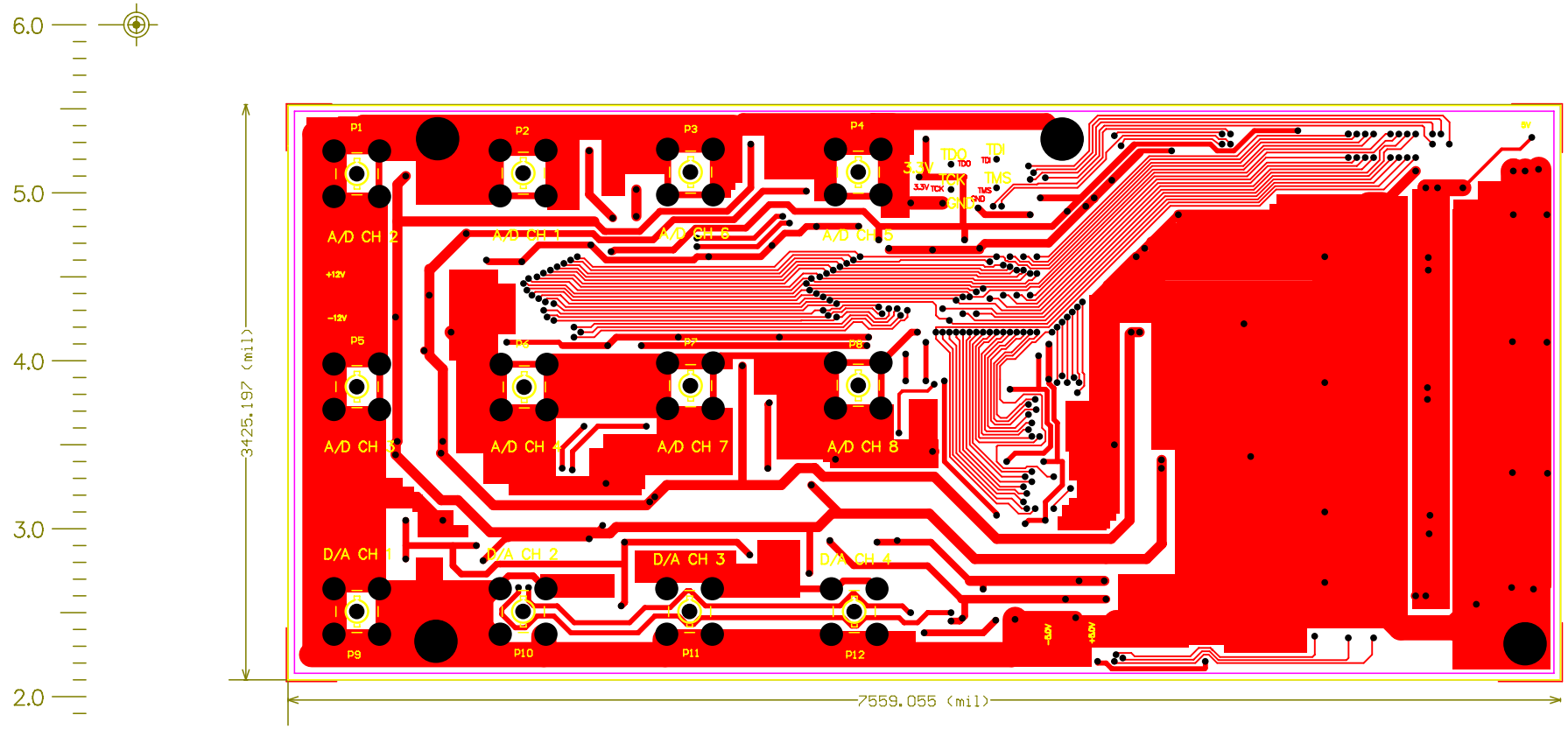
Size: Letter
Scale: 1:1
Date 2005.04.25
Rev. 1
Sheet 1 of 4


+2.500V
3.3V
C37
100nF
3.3V / 5V
U14
+5.0V
C38
100nF
D15
D14
D13
D12
D11
D10
D9
D8
74LVXC3245
D[0..15]
C54
100nF
C53
100nF
U16
D7
D6
D5
D4
D3
D2
D1
D0
74LVXC3245
C70
100nF
C69
100nF
U22
RESET#
LOADDACS#
R/W#
A1
A0
CS_DAC#
74LVXC3245
3.3V / 5V
-2.500V
+2.500V
C36
100nF
U13
OPA2277
-5.0V
C30
100nF
U19
DAC7644
DB15
DB14
DB13
DB12
DB11
DB10
DB9
DB8
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
RSTSEL
RST
LOADDACS
R/W#
A1
A0
CS_
DGND
NC
V OUTA Sense
V OUTA
V REFL AB Sense
V REFL AB
V REFH AB
V REFH AB Sense
V OUTB Sense
V OUTB
V OUTC Sense
V OUTC
V REFH CD Sense
V REFH CD
V REFL CD
V REFL CD Sense
V OUTD Sense
V outD
V SS
AGND
V CC
V DD
C59
330pF
C52
330pF
C78
330pF
C81
330pF
C77
100nF
2.2uF
C75
C94
100uF
C76
2.2uF
C93
100uF
C92
100nF
U25
C91
100nF
R23
10k0
R19
10k0
U17
BUF634U
C58
2.2uF
U18
OPA2277
C72
2.2uF
C51
2.2uF
C67
2.2uF
C46
22uF
C47
22uF
P9
BNC
CH 1
-5V...+5V
R24
10k0
R25
10k0
U26
BUF634U
C90
2.2uF
C71
2.2uF
P10
BNC
CH 2
-5V...+5V
R26
10k0
R22
10k0
U24
BUF634U
C61
2.2uF
U20
OPA2277
C68
2.2uF
C73
2.2uF
C88
2.2uF
C74
22uF
C65
22uF
P11
BNC
CH 3
-5V...+5V
R28
10k0
R27
10k0
U27
BUF634U
C89
2.2uF
C86
2.2uF
P12
BNC
CH 4
-5V...+5V
+12.0V
-12.0V
aSoos Inc.
Title
A2D2A - D/A Conversion
Size: Letter
Scale: 1:1
Date 2005.04.25
Rev. 1
Sheet 2 of 4


J2
PERIPHERAL CONNECTOR
DSK6711
J1
MEMORY CONNECTOR
DSK6711
U4
EPM7032AE
CS2->CS#
EA2->A0
EA4->A2
EA5->A3
EA3->A1
TIN
INT4
RESET#
ARE#
AOE#
AWE#
D0
D1
A0
A1
WR#
RD#
CONVST#
FRSDATA1
BUSY1
CS_ADC1#
FRSDATA2
BUSY2
CS_ADC2#
LOADDACS#
R/W#
CS_DAC#
TDI
TDO
TMS
TCK
D[0..15]
C1 100nF
C8 100nF
C14 100nF
C15 100nF
5V
3.3V
aSoos Inc.
A2D2A - DSP Interface
Size: Letter
Scale: 1:1
Date 2005.04.25
Rev. 1
Sheet 3 of 4


CH 8
CH 7
CH 6
CH 5
CH 4
CH 3
CH 2
CH 1
P8 BNC
P7 BNC
P3 BNC
P4 BNC
P6 BNC
P5 BNC
P1 BNC
P2 BNC
U11
U2
U8
U3
OPA2277
C40 100nF
C35 100nF
C4 100nF
C5 100nF
C39 100nF
C34 100nF
C3 100nF
C6 100nF
-12.0V
+12.0V
U7
U6
AD7865
AGND
V IN4B
V IN4A
V IN3B
V IN3A
V IN2B
V IN2A
V IN1B
V IN1A
STBY_
H_/S SEL
SL4
SL3
CLK/SL2
CLK IN/SL1
WR#
RD#
CS#
CONV#
FRSDATA
BUSY
EOC_
DB 0
DB 1
DB 2
DB 3
DB 4
DB 5
DGND
VDRIVE
DVDD
DB 6
V REF
A VDD
INT_/EXT
C13 330pF
C11 330pF
C9 2.2uF
C12 2.2uF
C20 100nF
C10 100nF
C19 100nF
C18 100nF
+5.0V
3.3V
D2
D3
D4
D5
D6
D7
D0
D1
D8
D9
D10
D11
D12
D13
D14
D15
CS_ADC2#
FRSDATA2
BUSY2
WR#
RD#
CONVST#
D[0..15]
CS_ADC1#
FRSDATA1
BUSY1
+2.5V_B
+2.5V_A
C7 100nF
C2 100nF
U1
-5.0V
+2.500V
aSoos Inc.
Title
A2D2A - A/D Conversion
Size: Letter
Scale: 1:1
Date 2005.04.25
Rev. 1
Sheet 4 of 4



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ENGINEER: PHONE:	PART NO.: 20020907	REV: 1	DATE: 2005.04.25
FILE NAME: A2D2A	LAYER: 2	GERBER: .GTS	

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	ENGINEER: Soos, Antal PHONE: (403)228-2842
	ENGINEER: PHONE:
DATE: 2005.04.25	REV: 1
	PART NO.: 20020907
FILE NAME: A2D2A	LAYER: 2
GERBER: .GBS	